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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,750	03/15/2001	Huy Thanh Vo	303.723US1	4340

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
MAI, SON LUU	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,750	VO, HUY THANH	
	Examiner	Art Unit	
	Son L. Mai	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02-24-2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02-24-03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanoi (U.S. Patent 5,708,621).

Regarding claims 1, 8, 15, 26, 30, 42 and 45, Tanoi discloses a memory array (1 in fig. 1) comprising: a number of memory cells (6) having a first source/drain region and a second source/drain region and a gate region (parts of an access transistor in a dynamic random access memory); a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (4) coupled to the second source/drain region of at least one memory cell; a number of wordlines (2)

coupled to the gate region of at least one memory cell; a strapping line (118 in fig. 16) of lower resistance than the wordlines coupled to a single wordline wherein the strapping line bypasses a portion of the single wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch (fig. 18); and at least two channels (122, 126 in fig. 18) connecting the strapping line to a first and second end of the portion of the single wordline.

Regarding claims 2, 3, 6, 7, 9, 10, 16, 17, 20, 21, 27, 28, 31, 32, 39, 44, 46, 47, 50, 51, Tanoi teaches at column 7, lines 54-57, the strapping lines comprise metal.

Regarding claims 4, 29, Tanoi shows in figure 16, the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline.

Regarding claims 5, 19, 37 and 49, Tanoi teaches a memory array, comprising: a number of memory cells having a first source/drain region and a second source/drain region and a gate region (parts of an access transistor in a dynamic random access memory); a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (4 in fig. 1) coupled to the second source/drain region of at least one memory cell; a number of wordlines (2 in fig. 1) coupled to the gate region of at least one memory cell; a plurality of strapping lines (50 in fig. 4) of lower resistance than the wordlines coupled to at least one of the number of wordlines wherein the strapping lines (lines 50 consisting of two strapping lines joining at interconnecting plug 60) bypass a plurality of portions (54, 56) of a single wordline;

and a plurality of channels (60 in fig. 6) connecting the plurality of strapping layers to the wordline.

Regarding claims 11, 22, 33, Tanoi shows in figure 4, the portions (38, 40, 42) of the wordlines (37) in the array bypassed by the number of strapping devices (line 36 has 2 portions) comprises a plurality of end portions (44, 46,48) of the wordlines.

Regarding claims 12, 23, 34, 52, Tanoi shows in figure 4, the strapping devices are located on alternating wordlines in the array.

Regarding claims 13, 24, 35, 53, Tanoi shows in figure 16, the strapping devices (108, 118) are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

Regarding claims 14, 18, 25, 36, 54, Tanoi shows in figure 16, the strapping devices (108, 118) strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines.

Regarding claims 38, 43, the method of reducing a wordline RC time constant reads on figure 16 of Tanoi, wherein activating a second number of transistors coupled to a second portion (114) of a wordline comprises: sending a signal through a first channel(112) to a metal strapping line(108); sending the signal through the metal strapping line; and sending the signal through a second channel (116) to the second portion(114) of the wordline.

Regarding claim 40, the method of reducing a wordline RC time constant as claimed reads on figure 16 wherein activating a first number of transistors coupled to a

first portion (110) of a wordline comprising activating a first number of transistors coupled to a first half of the wordline.

Regarding claims 41, 48, the method of reducing a wordline RC time constant reads on figure 4, wherein activating a selected row in a memory array comprises bypassing multiple portions (38, 40) of the wordline (37) using multiple strapping devices (strapping line 36 has 2 portions connecting at interconnecting plug 46) of lower resistance than the wordline.

Tanoi does not explicitly depict a width of the strapping line being greater than a width of the wordlines as now included in the independent claims 1, 5, 8, 15, 19, 26, 30, 37, 42, 45 and 49. As is well-known in the art, a wider conductor has lower resistance. Tanoi shows in one embodiment in figures 16-18, a strapping line 118 having low resistance (column 9, lines 33-41) and gaps between the strapping lines are large to accommodate wider strapping lines. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the strapping lines wider to lower resistance of the strapping lines and to reduce propagation delay of the strapping lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 305-3497. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 308-4910. The fax phone numbers for the

organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

03-05-2003

Son L. Mai
Primary Examiner
Art Unit 2818